**Global Research Outreach\_2025\_Call for Proposal**

**Theme: System Architecture**

**- Sub-Theme: System Semiconductor Design with Agentic AI**

Agentic AI such as ChipAgents, AiEDA, and Chipmind has emerged as a game-changer in semiconductor chip design, significantly enhancing both design precision and speed. Eventually, the focus will shift toward developing AI agents capable of delivering integrated designs from digital to analog domains, ultimately boosting the overall productivity.

To move beyond traditional ML-based tools confined only to specific design stages, our aim is to create an end-to-end semiconductor design automation system encompassing spec input, schematic generation, layout design, GDS file extraction, multi-silicon integration, and packaging optimization. We expect that automated Analog/Digital circuit design frameworks will reduce the Turn-Around-Time (TAT) and optimize the Power, Performance, Area (PPA) design more thoroughly. Moreover, it will also facilitate heterogeneous circuit designs (e.g., analog/digital co-design), which are currently very difficult to achieve.

We thus look for innovators in ***Agentic AIs*** and ***Automated Semiconductor Designs*** who can contribute to this challenging project. Proposals should detail feasibility studies and projected outcomes in areas such as but not limited to:

* Analog Circuit Synthesis: Synthesize high-performance analog circuits by optimizing critical parameters such as gain, bandwidth, and noise margins.
* Cross-Node Circuit Design Migration: Expedite the migration of digital or analog circuit designs across diverse process nodes, automating device updates and parameter adjustments.
* Layout Optimization: Refine analog layouts to minimize parasitic effects and ensure maximum signal integrity.
* Mixed-Signal Co-design: Handle simultaneous analog and digital design challenges, enabling efficient heterogeneous circuit integration.
* Defect Detection and Diagnosis: Identify anomalies in analog designs during the early stages of development, minimizing iteration cycles and associated costs.
* Verification and Validation: Validate designs against specifications to ensure reliability and compliance prior to fabrication.

※ *The topics are not limited to the above examples and the participants are*

 *encouraged to propose the original idea.*

※ *Funding: Up to USD 150,000 per year*