Theme: Semiconductor Process

- Sub Theme: Sub-10nm, High Aspect Ratio Trench Etching Technique

Recently, High Aspect-Ratio Trench (HART) in patterning at the 10nm level, in particular, is an essential processing etch skill that enables the fabrication of semiconductor devices such as DARM, VNAND, and LOGIC devices. HARTs are also necessary to achieve large values of capacitance in the fabrication of charge storage capacitors in DRAM devices. Etching of HART suffers from the inherent RIE lag mechanism caused by reduced energy of ions and the number of etching species at the bottom of a deep trench. As a result, the process difficulty in plasma etching has significantly increased, and more precise process control and advanced etch technologies are required to form a fine pattern

The topics we are through this GRO are as follows:

- · High Aspect Ratio (HAR)Silicon patterning at the 10nm level including at cryogenic conditions (A/R >3.9)
- · Repeatability enhanced high-temperature sensor for multiple equipment
- · In-situ calibrated or calibration-less non-contact high-temperature sensor
- · Depth Loading Minimization Technology for various SPACEs from 9.5 to 30nm
- · Mask Selectivity [Oxide] >5.8
- · Leaning Free Trench Patterning

※ *The topics are not limited to the above examples and the participants are encouraged to propose the original idea.*

※ *Funding: Up to USD 150,000 per year*