Theme: Electric Material

- Sub Theme: New Materials

The semiconductor scaling is leading to the metal interconnect width of less than 10 nm diameter and results in high resistance and RC delay. To overcome the RC signal-delay in the down-scaling of electronics, the development of low-resistance metal interconnects and mechanically-robust ultra low-k dielectric materials are required

From this perspective, the requirements for the candidates are as follows:

1. alternative Metal interconnect (superior to Cu, Co, Ru) which has low resistivity at nanoscale dimensions and compatibility with the CMOS process.

2. ULK dielectric material with extreme low-k (k<2.0) and sufficient mechanical properties (Young's modulus>10GPa), or A new material with excellent mechanical properties (Young's modulus >80GPa) and sufficient low-k (k<3.0).

We welcome the idea of new electronic materials, except for the sub-themes from 2-1 to 2-5 as we listed.

※ *The topics are not limited to the above examples and the participants are encouraged to propose the original idea.*

※ Funding: Up to USD 150,000 per year