SAMSUNG

Theme: Semiconductor Process

- Sub-theme: Ultrathin, High-Quality SiO_2 for Extremely Large Surface Area

Next-generation semiconductor devices including sub-10nm conventional and 3-dimensional DRAMs strongly demand ultrathin, high quality SiO2-based dielectric technologies for cell transistors. Since the traditional oxidation processes consume ~46% of silicon substrate after oxide formation, which results in the shortage of active area, the deposition of thin SiO2 and subsequent curing processes are prevailing in recent conventional DRAMs. Furthermore, 3-dimensional DRAMs are expected to require lateral step coverage of dielectric films, which provides highly conformal deposition and surface treatments including oxidation and nitridation for ultra-large surface area. We are aiming to explore novel technologies for ultrathin(≤30Å), high quality oxidation, and nitridation technologies providing low silicon consumption(≤3Å) covering the extremely large surface area for sub-10nm and 3D DRAMs.

The topics we pursue through this GRO are as follows:

- Ultrathin(≤30Å), but highly reliable SiO2-based gate dielectric technologies including oxidation and nitridation provide low silicon consumption(≤3Å) and high conformality.
- Innovative oxidation and nitridation processes and systems for ultrathin gate dielectrics

※ *The topics are not limited to the above examples and the participants are encouraged to propose the original idea.*

※ *Funding: Up to USD 150,000 per year*