Theme: Semiconductor Process

- Sub Theme: 3D Monolithic Integration

The dimensional scaling-down principle of silicon transistor enables semiconductor technology to conquer the entire industrial field gradually or fastly. The various vertical transistors have been developed and adopted as the cutting-edge technology such as FinFET, GAAFET, MBCFET, and VNAND to avoid the conventional planar shrinkage wall.

We aim furtherly to contribute to the next boost idea creation of scientific invention in terms of 3D monolithic integration. Practically, the conceptual demonstration will not confine the individual memory and logic application. Sequential integration on top of the same starting substrate would be considered a good candidate as an example of a monolithic 3DIC composed of functional layers of logic and memory.

The topics we pursue through this GRO are as follows:

- Low Temperature Transistor Technology
- Low Temperature (below 450C) Si layer transfer Process, which has no mobility degradation
- Low Resistance & Reliable BEOL Interconnection at 450C or less

※ *The topics are not limited to the above examples and the participants are encouraged to propose the original idea.*

※ *Funding: Up to USD 150,000 per year*