Theme: Semiconductor Process

- Sub Theme: Thermal management solutions

As Moore's Law transistor scaling has been slowing down in recent years, an ongoing effort has been made to put more transistors into single chips and 2.5/3D heterogeneous integration has become one of the most important alternatives in post-Moore's Law era. With the increase of device integration density and the complexity of chip function design, major semiconductor foundries has turned to offer advanced single and multi-chip packaging solutions. However, for the multiple chips within a chip stack, the increase of power density caused heat dissipation difficulties, which has a considerable impact on the design of chip and integration system function and stability. Therefore, to effectively control the excessive heat generated by multiple chips, thermal analysis and management are crucial for next-gen heterogeneously integrated 2.5/3D IC designs.

We are highly interested in (but not limited to) the following list of topics.

- Cooling solutions for high performance computing (HPC) devices (e.g. two-phase cooling, direct liquid cooling, immersion cooling, etc.)
- Embedded cooling structures eliminating most sequential thermal resistance from the chip to the ambient, unlike cold plates/heat sinks
- Co-designing electronics and die-embedded microchannel that we can build a monolithically integrated manifold microchannel cooling structure
- Evaporation and boiling heat transfer on micro/nanostructured surfaces with excellent wicking capability
- Materials ensuring high reliability enabling liquid or liquid-vapor cooling within packaging

※ *The topics are not limited to the above examples and the participants are encouraged to propose the original idea.*

※ *Funding: Up to USD 150,000 per year*